LF155/LF156/LF256/LF257/LF355/LF356/LF357 JFET Input Operational Amplifiers

Check for Samples: LF155, LF156, LF355, LF356, LF357

FEATURES

Advantages

- **Replace Expensive Hybrid and Module FET Op Amps**
- **Rugged JFETs Allow Blow-Out Free Handling Compared with MOSFET Input Devices**
- **Excellent for Low Noise Applications Using Either High or Low Source Impedance—Very Low 1/f Corner**
- **Offset Adjust Does Not Degrade Drift or Common-Mode Rejection as in Most Monolithic Amplifiers**
- **New Output Stage Allows Use of Large Capacitive Loads (5,000 pF) without Stability Problems**
- **Internal Compensation and Large Differential Input Voltage Capability**

APPLICATIONS

- **Precision High Speed Integrators**
- **Fast D/A and A/D Converters**
- **High Impedance Buffers**
- **Wideband, Low Noise, Low Drift Amplifiers**
- **Logarithmic Amplifiers**
- **Photocell Amplifiers**
- **Sample and Hold Circuits**

DESCRIPTION

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

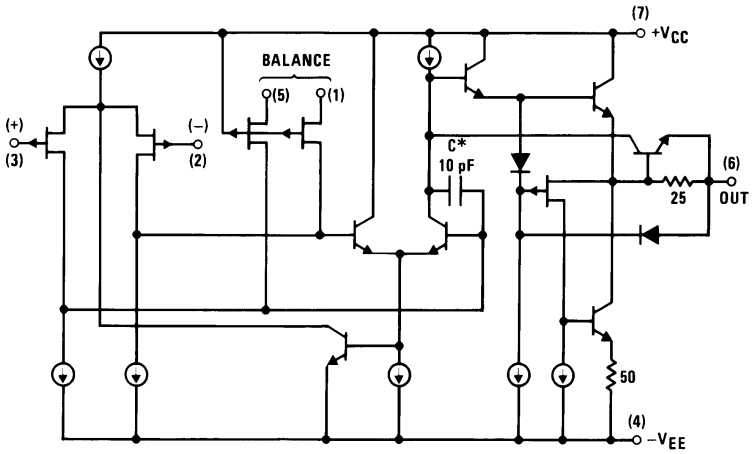
Common Features

- Low Input Bias Current: 30pA
- Low Input Offset Current: 3pA
- High Input Impedance: $10^{12}\Omega$
- Low Input Noise Current: 0.01 pA/$\sqrt{\text{Hz}}$
- High Common-Mode Rejection Ratio: 100 dB
- Large DC Voltage Gain: 106 dB

Table 1. Uncommon Features

	LF155/ LF355	LF156/ LF256/ LF356	LF257/ LF357 (A_V=5)	Units
Extremely fast settling time to 0.01%	4	1.5	1.5	µs
Fast slew rate	5	12	50	V/µs
Wide gain bandwidth	2.5	5	20	MHz
Low input noise voltage	20	12	12	nV / $\sqrt{\text{Hz}}$

Simplified Schematic



*3pF in LF357 series.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

	LF155/6	LF256/7/LF356B	LF355/6/7
Supply Voltage	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±30V
Input Voltage Range [3]	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous
T_{JMAX}			
LMC Package	150°C	115°C	115°C
P Package		100°C	100°C
D Package		100°C	100°C
Power Dissipation at T_A = 25°C [1] [4]			
LMC Package (Still Air)	560 mW	400 mW	400 mW
LMC Package (400 LF/Min Air Flow)	1200 mW	1000 mW	1000 mW
P Package		670 mW	670 mW
D Package		380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}			
LMC Package (Still Air)	160°C/W	160°C/W	160°C/W
LMC Package (400 LF/Min Air Flow)	65°C/W	65°C/W	65°C/W
P Package		130°C/W	130°C/W
D Package		195°C/W	195°C/W
(Typical) θ_{JC}			
LMC Package	23°C/W	23°C/W	23°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Soldering Information (Lead Temp.)			
TO-99 Package			
Soldering (10 sec.)	300°C	300°C	300°C
PDIP Package			
Soldering (10 sec.)	260°C	260°C	260°C
SOIC Package			
Vapor Phase (60 sec.)		215°C	215°C
Infrared (15 sec.)		220°C	220°C
ESD tolerance			
(100 pF discharged through 1.5kΩ)	1000V	1000V	1000V

(1) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D=(T_{JMAX}-T_A)/\theta_{JA}$ or the 25°C P_{dMAX}, whichever is less.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(3) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(4) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside specified limits.

DC Electrical Characteristics

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=50Ω, T_A=25°C		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=50Ω		5			5			5		µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S=50Ω, (2)		0.5			0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	T_J=25°C, (1) (3)		3	20		3	20		3	50	pA
		$T_J \leq T_{HIGH}$			20			1			2	nA
I_B	Input Bias Current	T_J=25°C, (1) (3)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	T_J=25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	50	200		50	200		25	200		V/mV
		V_O=±10V, R_L=2k										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k	±12	±13		±12	±13		±12	±13		V
		V_S=±15V, R_L=2k	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15.1		±11	±15.1		+10	+15.1		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(4)	85	100		85	100		80	100		dB

(1) Unless otherwise stated, these test conditions apply:

	LF155/156	LF256/257	LF356B	LF355/6/7
Supply Voltage, V_S	±15V ≤ V_S ≤ ±20V	±15V ≤ V_S ≤ ±20V	±15V ≤ V_S ±20V	V_S= ±15V
T_A	−55°C ≤ T_A ≤ +125°C	−25°C ≤ T_A ≤ +85°C	0°C ≤ T_A ≤ +70°C	0°C ≤ T_A ≤ +70°C
T_{HIGH}	+125°C	+85°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

(2) The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5µV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

(3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta_{JA}$ Pd where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(4) Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

DC Electrical Characteristics

$T_A = T_J$ = 25°C, V_S = ±15V

Parameter	LF155		LF355		LF156/256/257/356B		LF356		LF357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	10	mA

AC Electrical Characteristics

$T_A = T_J = 25°C$, $V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155/355	LF156/256/356B	LF156/256/356/LF356B	LF257/357	Units
			Typ	Min	Typ	Typ	
SR	Slew Rate	LF155/6: A_V=1,	5	7.5	12		V/µs
		LF357: A_V=5				50	V/µs
GBW	Gain Bandwidth Product		2.5		5	20	MHz
t_s	Settling Time to 0.01%	(1)	4		1.5	1.5	µs
e_n	Equivalent Input Noise Voltage	R_S=100Ω					
		f=100 Hz	25		15	15	nV/√Hz
		f=1000 Hz	20		12	12	nV/√Hz
i_n	Equivalent Input Current Noise	f=100 Hz	0.01		0.01	0.01	pA/√Hz
		f=1000 Hz	0.01		0.01	0.01	pA/√Hz
C_{IN}	Input Capacitance		3		3	3	pF

(1) Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF357, A_V = −5, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit).

Typical DC Performance Characteristics

Curves are for LF155 and LF156 unless otherwise specified.

Input Bias Current

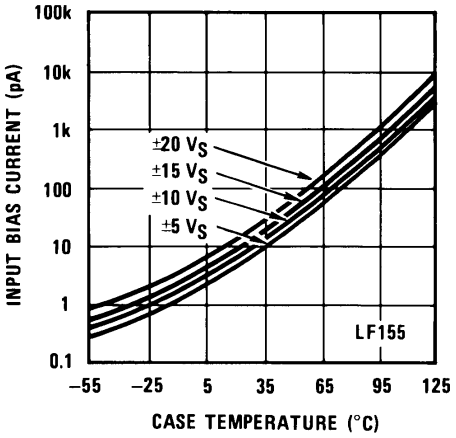


Figure 1.

Input Bias Current

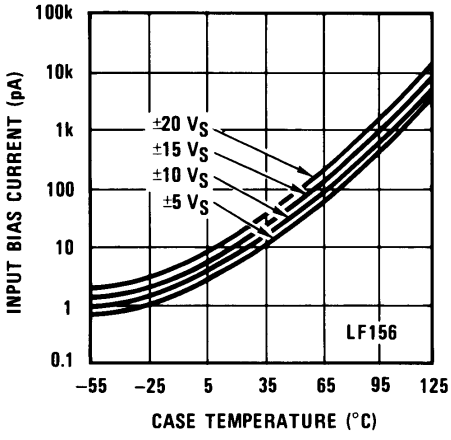


Figure 2.

Input Bias Current

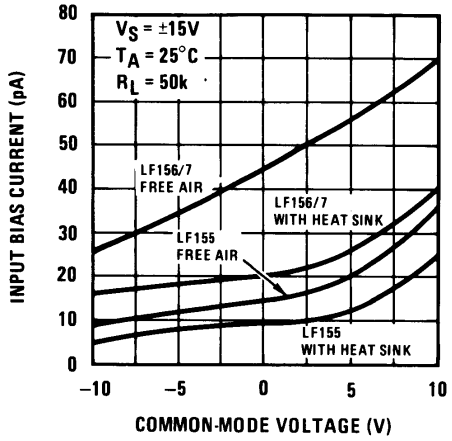


Figure 3.

Voltage Swing

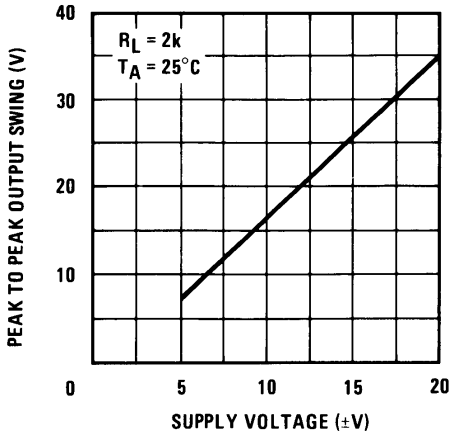


Figure 4.

Supply Current

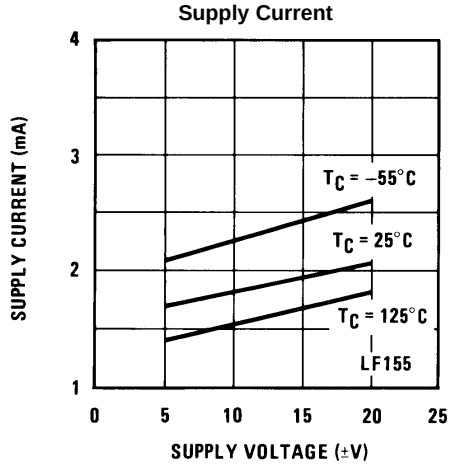


Figure 5.

Supply Current

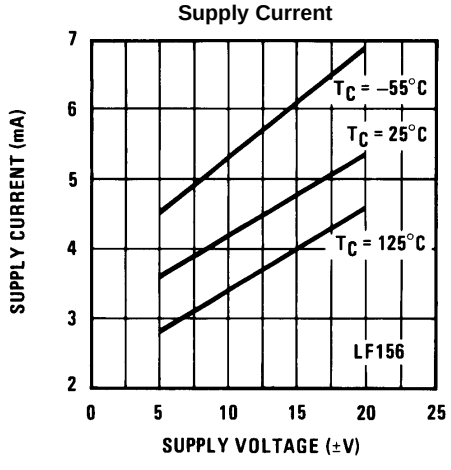


Figure 6.

Typical DC Performance Characteristics (continued)

Curves are for LF155 and LF156 unless otherwise specified.

Negative Current Limit

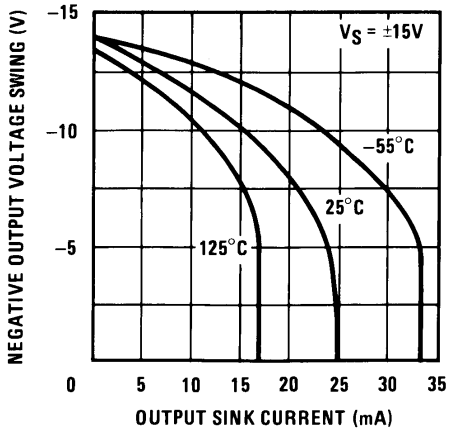


Figure 7.

Positive Current Limit

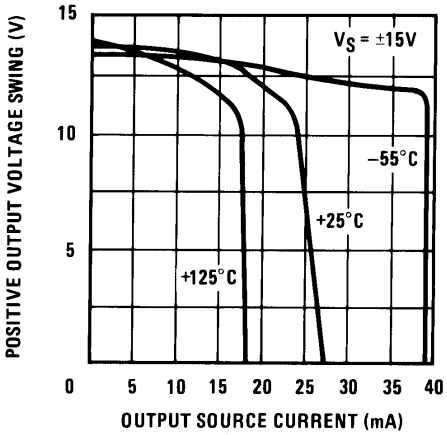


Figure 8.

Positive Common-Mode Input Voltage Limit

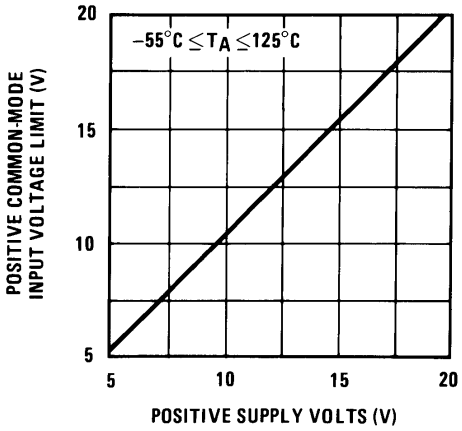


Figure 9.

Negative Common-Mode Input Voltage Limit

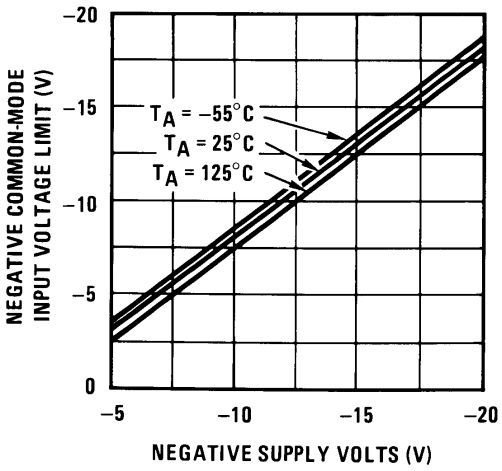


Figure 10.

Open Loop Voltage Gain

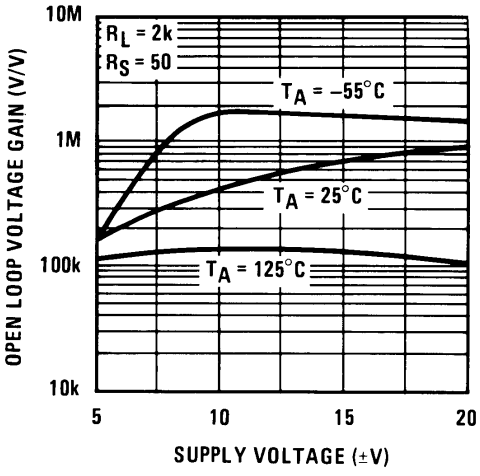


Figure 11.

Output Voltage Swing

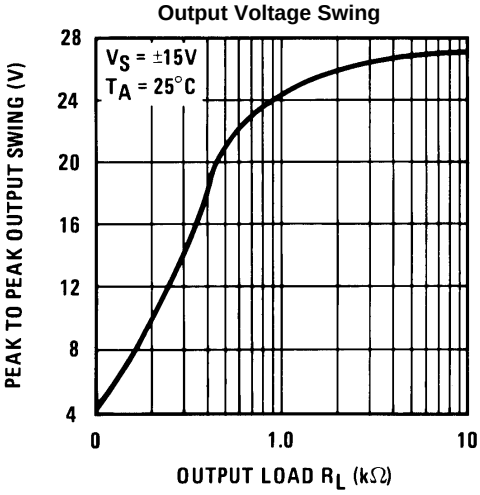


Figure 12.

Typical AC Performance Characteristics

Gain Bandwidth

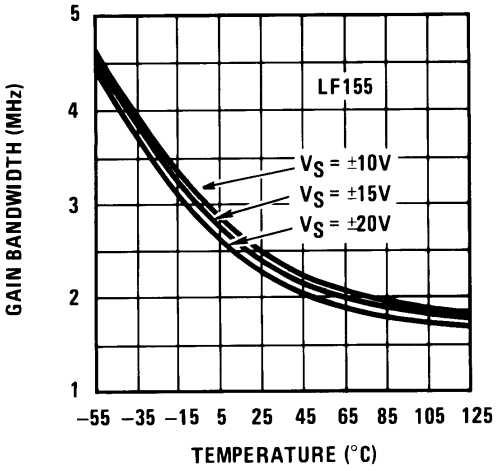


Figure 13.

Gain Bandwidth

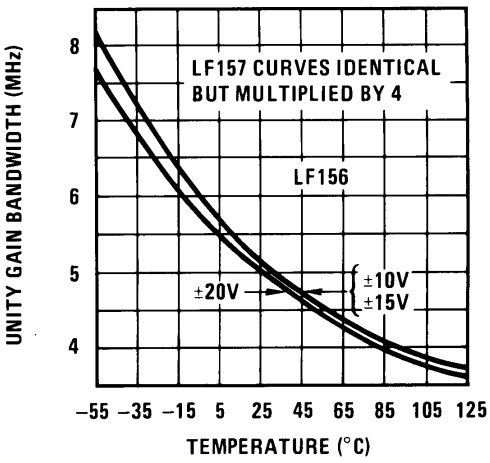


Figure 14.

Normalized Slew Rate

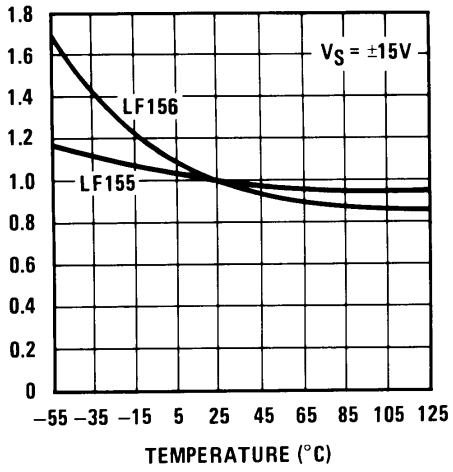


Figure 15.

Output Impedance

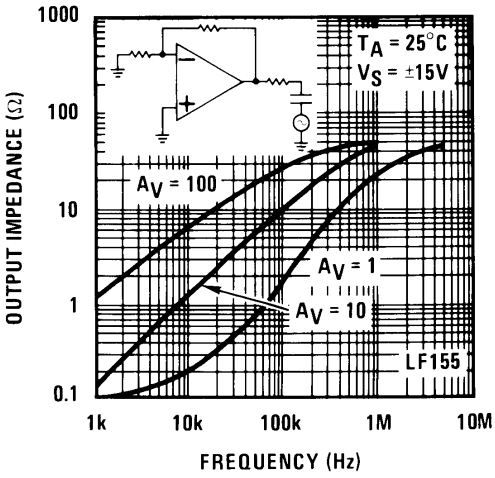


Figure 16.

Output Impedance

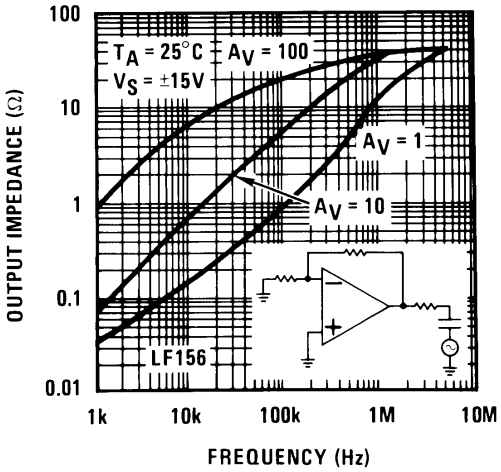


Figure 17.

Typical AC Performance Characteristics (continued)

LF155 Small Signal Pulse Response, A_V = +1

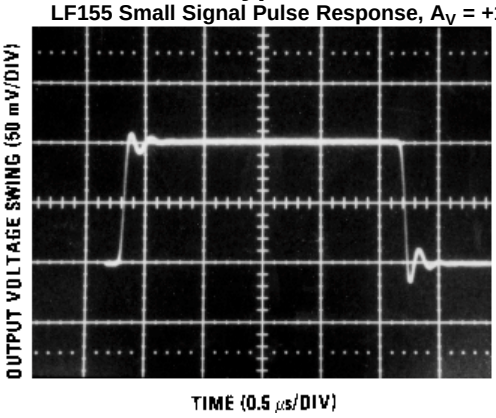


Figure 18.

LF156 Small Signal Pulse Response, A_V = +1

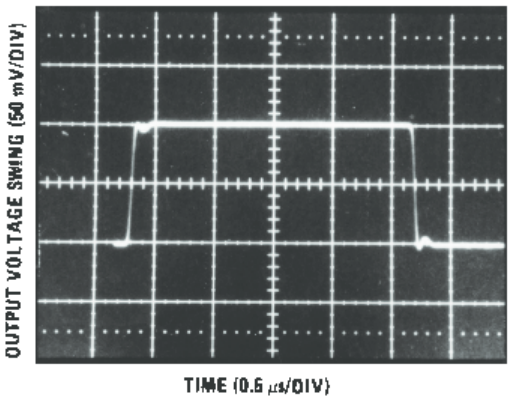


Figure 19.

LF155 Large Signal Pulse Response, A_V = +1

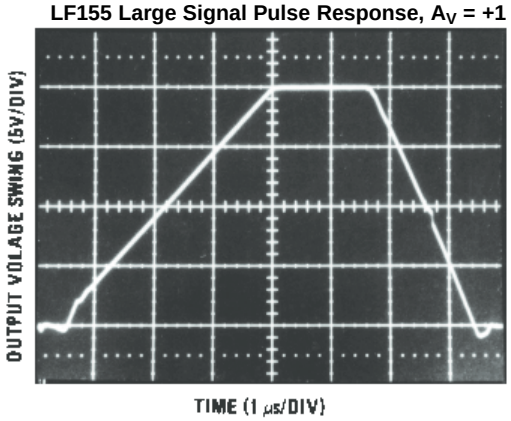


Figure 20.

LF156 Large Signal Puls Response, A_V = +1

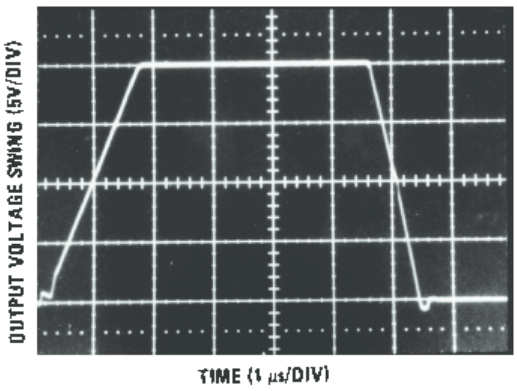


Figure 21.

Inverter Settling Time

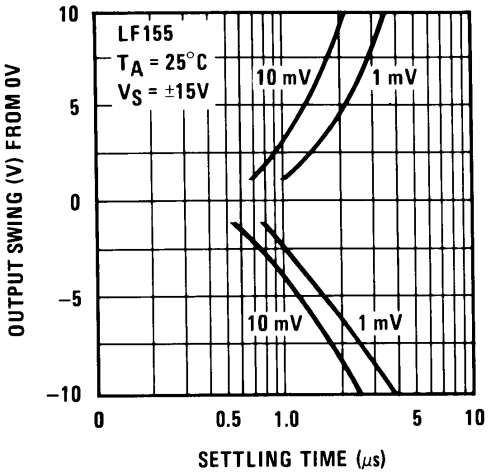


Figure 22.

Inverter Settling Time

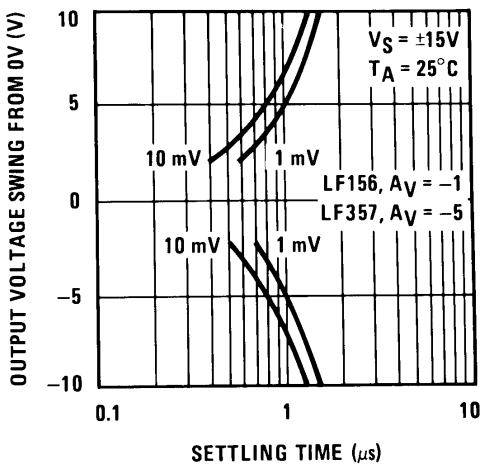


Figure 23.

Typical AC Performance Characteristics (continued)

Open Loop Frequency Response

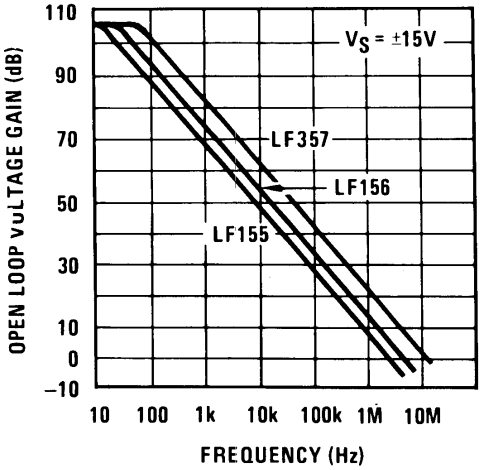


Figure 24.

Bode Plot

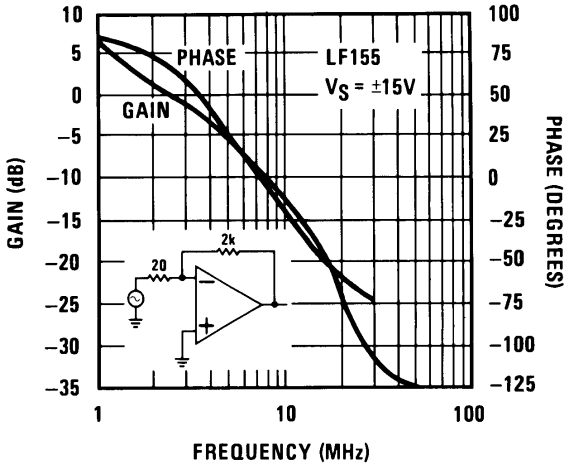


Figure 25.

Bode Plot

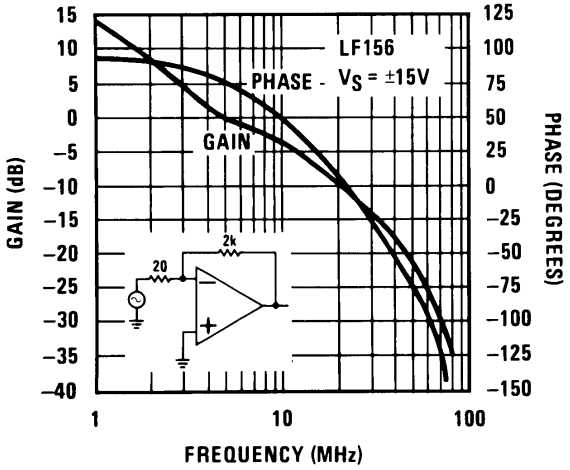


Figure 26.

Bode Plot

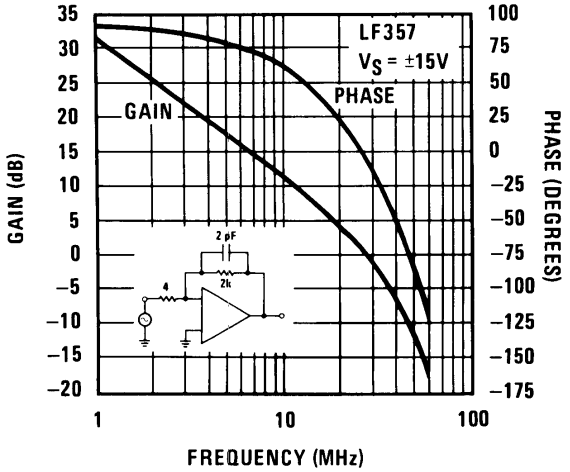


Figure 27.

Common-Mode Rejection Ratio

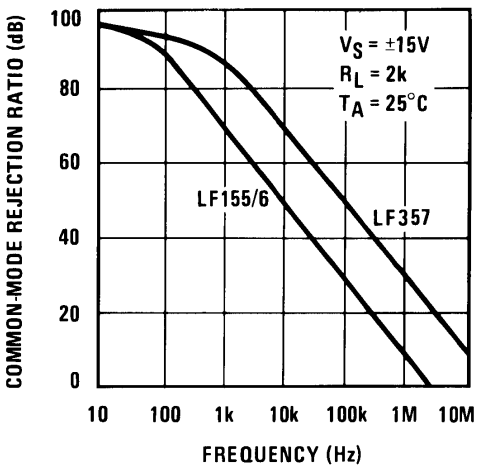


Figure 28.

Power Supply Rejection Ratio

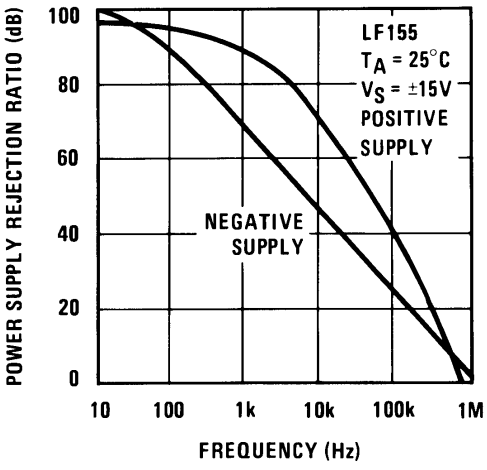


Figure 29.

Typical AC Performance Characteristics (continued)

Power Supply Rejection Ratio

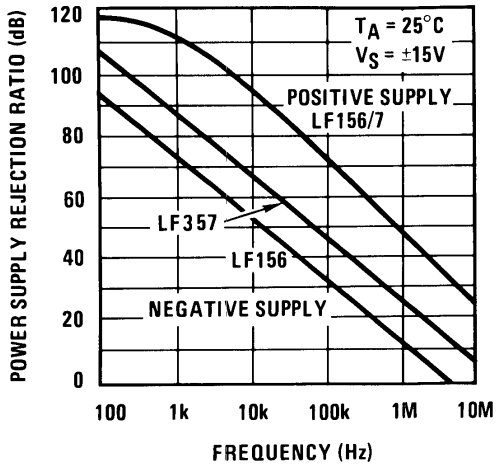


Figure 30.

Undistorted Output Voltage Swing

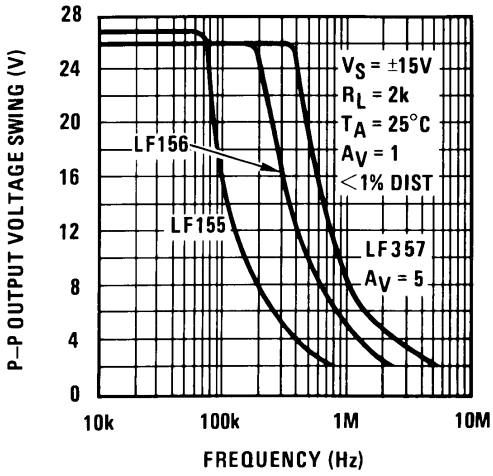


Figure 31.

Equivalent Input Noise Voltage

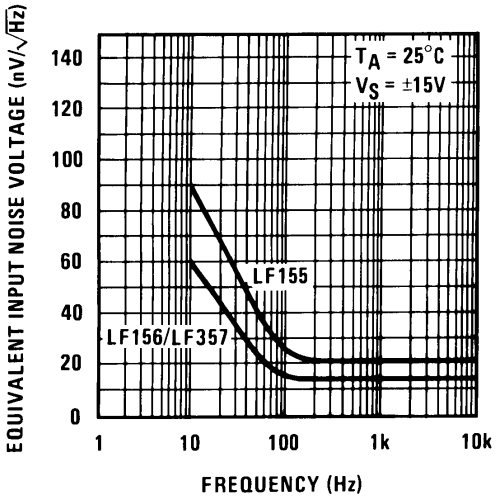


Figure 32.

Equivalent Input Noise Voltage (Expanded Scale)

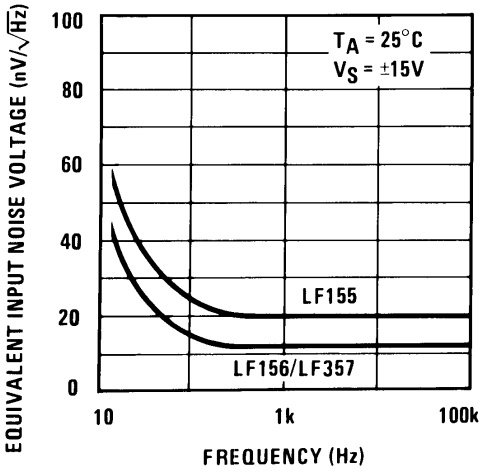
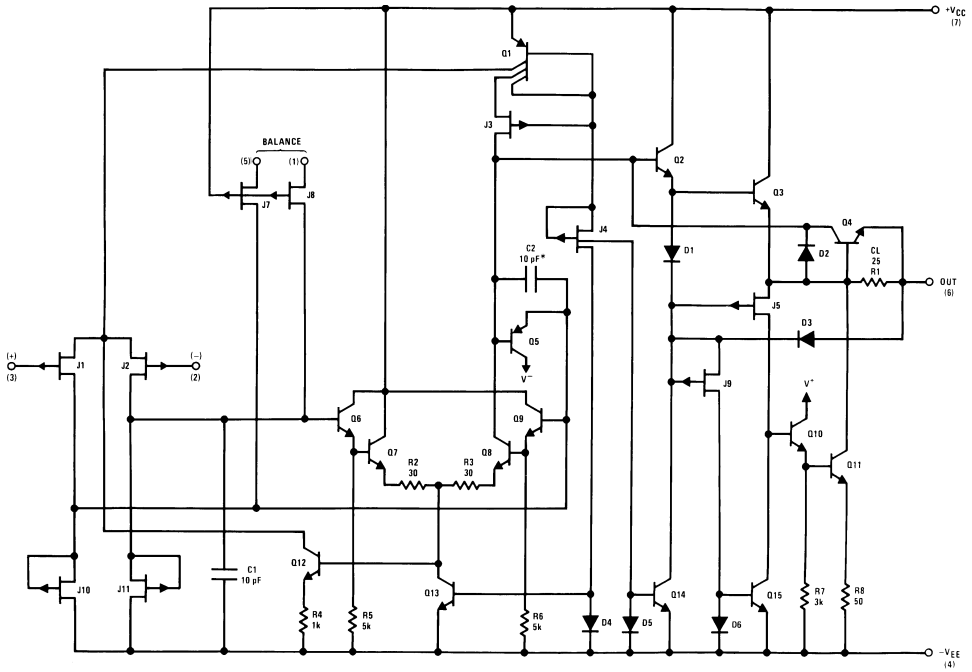


Figure 33.

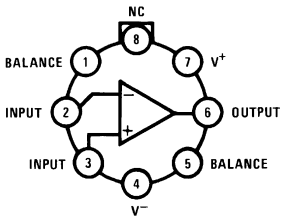
DETAILED SCHEMATIC



*C = 3pF in LF357 series.

Connection Diagrams

(Top Views)



*Available per JM38510/11401 or JM38510/11402

Figure 34. TO-99 Package (LMC)
See Package Number LMC (O-MBCY-W8)

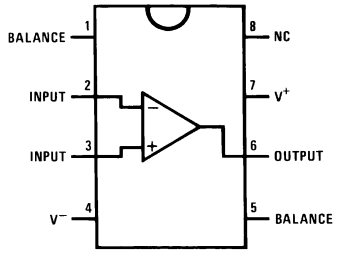


Figure 35. SOIC and PDIP Package (D and P)
See Package Number
D (R-PDSO-G8) or P (R-PDIP-T8)

APPLICATION HINTS

These are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pickup” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Circuit Connections

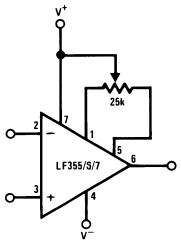
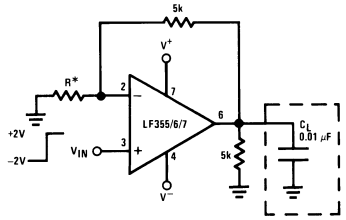


Figure 36. V_{OS} Adjustment

- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5µV/°C/mV of adjustment
- Typical overall drift: 5µV/°C ±(0.5µV/°C/mV of adj.)

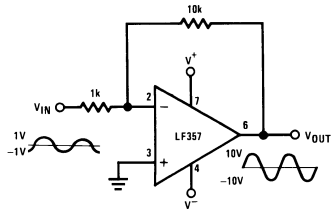


*LF155/6 R = 5k, LF357 R = 1.25k

Figure 37. Driving Capacitive Loads

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \approx 0.01\mu F$.

Overshoot ≤ 20%, Settling time (t_s) ≈ 5µs



For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500kHz.

Figure 38. LF357 - A Large Power BW Amplifier

Typical Applications

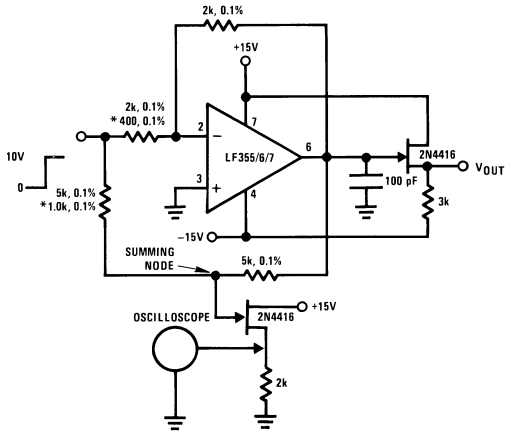


Figure 39. Settling Time Test Circuit

- Settling time is tested with the LF155/6 connected as unity gain inverter and LF357 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF357

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

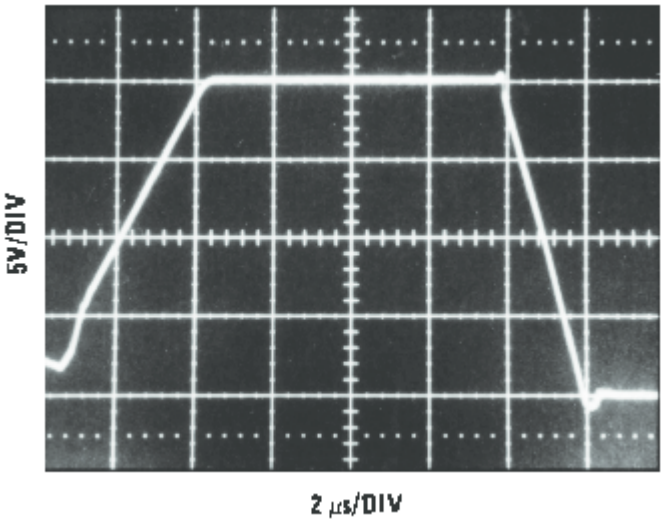


Figure 40. LF355

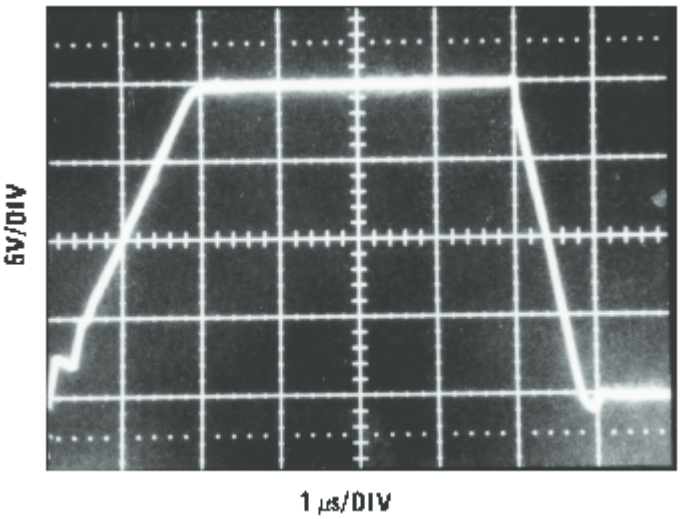


Figure 41. LF356

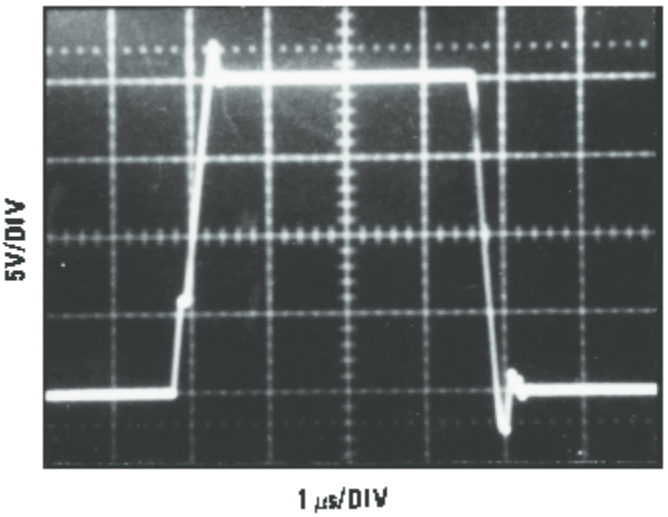


Figure 42. LF357

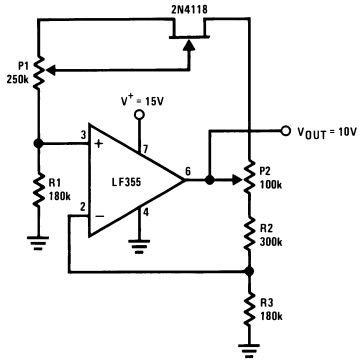


Figure 43. Low Drift Adjustable Voltage Reference

- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

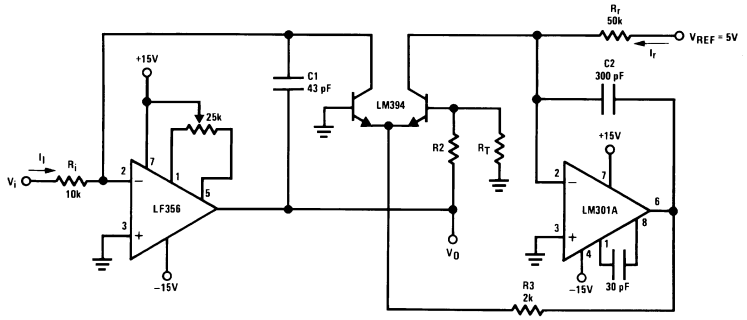


Figure 44. Fast Logarithmic Converter

- Dynamic range: 100µA ≤ I_i ≤ 1mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3µs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \text{ in } V_i \left[\frac{R_r}{V_{REF}\ Ri}\right] = \log V_i \frac{1}{R_i I_r} \quad R2 = 15.7k,\ R_T = 1k,\ 0.3\%/^{\circ}C \text{ (for temperature compensation)}$$

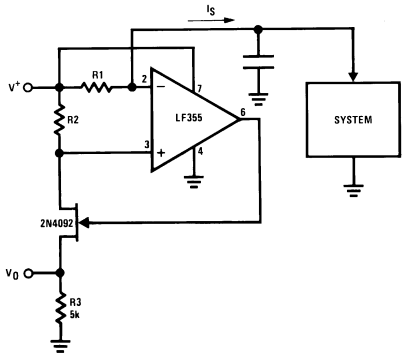


Figure 45. Precision Current Monitor

- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low I_B
  - Low V_{OS}
  - Low Supply Current

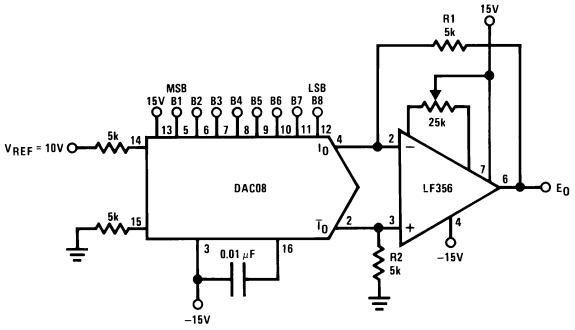
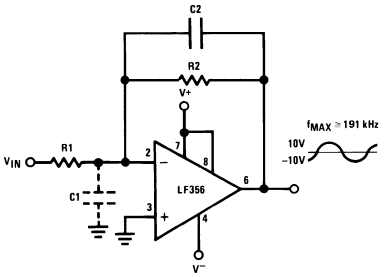


Figure 46. 8-Bit D/A Converter with Symmetrical Offset Binary Operation

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3µs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale



- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 191\,kHz$

Figure 47. Wide BW Low Noise, Low Drift Amplifier

- Parasitic input capacitance C1 ≃ (3pF for LF155, LF156 and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2 C2 ≃ R1 C1.

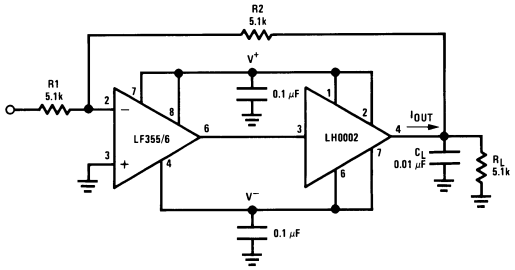
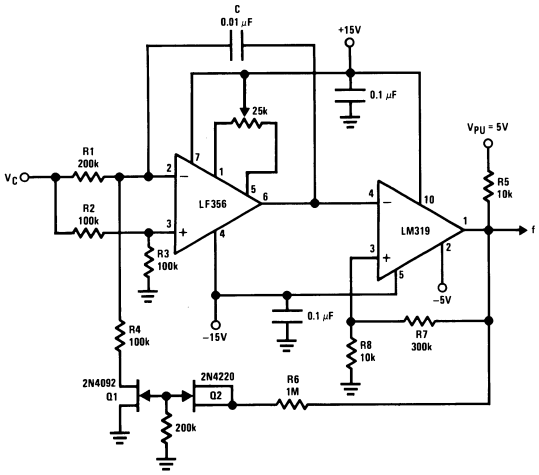


Figure 48. Boosting the LF156 with a Current Amplifier

- $I_{OUT(MAX)} \simeq 150mA$ (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}\ V/\mu s$ (with C_L shown)
- No additional phase shift added by the current amplifier



$$f = \frac{V_C (R8 + R7)}{(8\ V_{PU}\ R8\ R1)\ C'} \quad 0 \le V_C \le 30V,\ 10\,Hz \le f \le 10\,kHz$$

R1, R4 matched. Linearity 0.1% over 2 decades.

Figure 49. Decades VCO

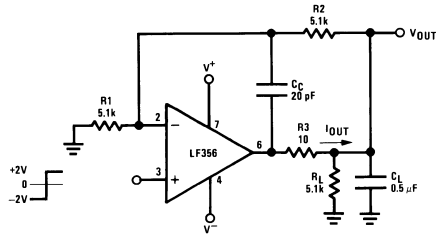


Figure 50. Isolating Large Capacitive Loads

- Overshoot 6%
- t_s 10µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s\ (\text{with } C_L \text{ shown})$$

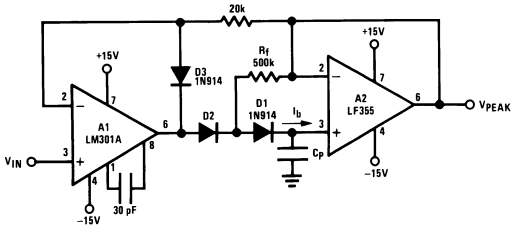
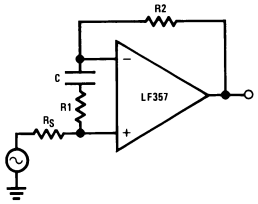


Figure 51. Low Drift Peak Detector

- By adding D1 and R_f, V_{D1}=0 during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of Cp.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN}-V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be << $\frac{1}{2}\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.



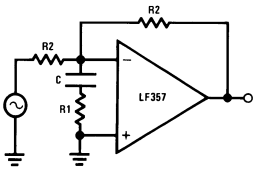
$$R1C \geq \frac{1}{(2\pi)\ (5\ MHz)}$$

$$R1 = \frac{R2 + R_S}{4}$$

$$A_{V(DC)} = 1$$

$$f_{-3\,dB} \approx 5\ MHz$$

Figure 52. Non-Inverting Unity Gain Operation for LF157



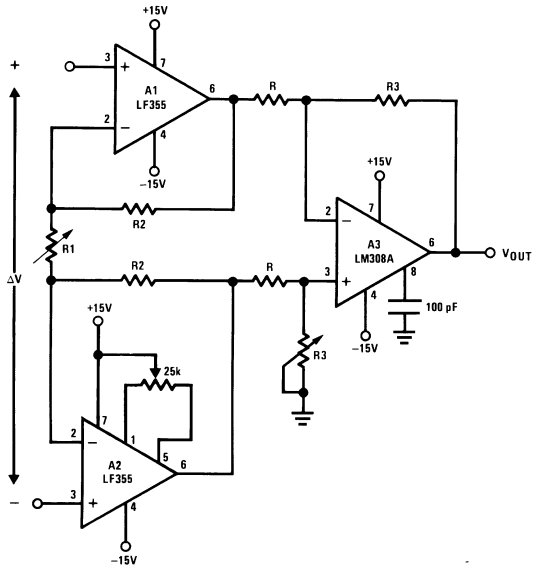
$$R1C \geq \frac{1}{(2\pi)\ (5\ MHz)}$$

$$R1 = \frac{R2}{4}$$

$$A_{V(DC)} = -1$$

$$f_{-3\,dB} \approx 5\ MHz$$

Figure 53. Inverting Unity Gain for LF157



• $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]\Delta V,\ V^- + 2V \leq V_{IN}\ \text{common-mode} \leq V^+$

Figure 54. High Impedance, Low Drift Instrumentation Amplifier

- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

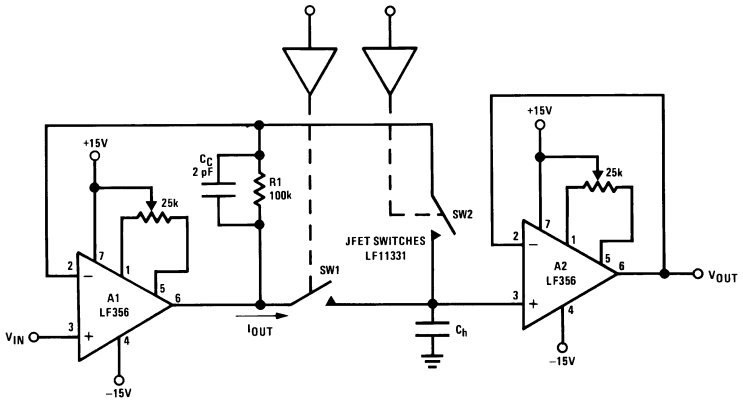


Figure 55. Fast Sample and Hold

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

$$T_A \cong \left[\frac{2R_{ON}, V_{IN}, C_h}{S_r}\right] 1/2 \text{ provided that:}$$

$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}, R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN} C_h}{20\ mA}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

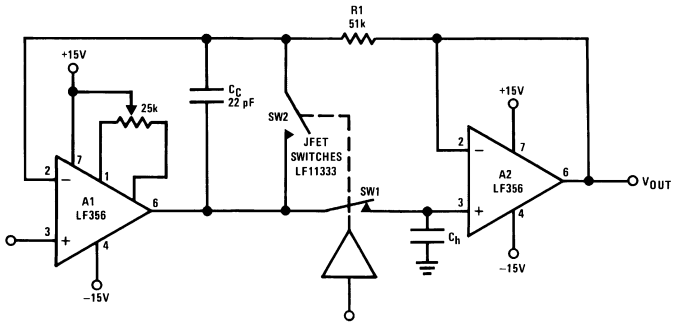


Figure 56. High Accuracy Sample and Hold

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1.
  - No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added
  - propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

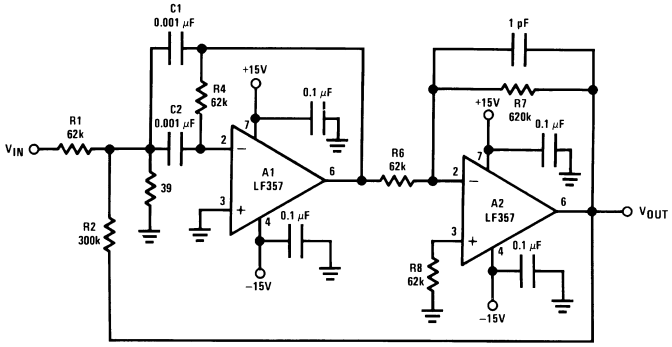


Figure 57. High Q Band Pass Filter

- By adding positive feedback (R2)
- Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1Vp-p tone burst: 300µs

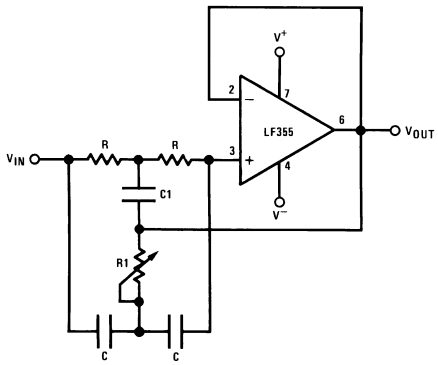


Figure 58. High Q Notch Filter

- 2R1 = R = 10MΩ
  - 2C = C1 = 300pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - Low I_B
  - Low supply current

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LF156H	ACTIVE	TO-99	LMC	8	500	TBD	Call TI	Call TI	-55 to 125	LF156H	Samples
LF156H/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LF156H	Samples
LF256H	ACTIVE	TO-99	LMC	8	500	TBD	Call TI	Call TI	-25 to 85	LF256H	Samples
LF256H/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	-25 to 85	LF256H	Samples
LF356H	ACTIVE	TO-99	LMC	8	500	TBD	Call TI	Call TI	0 to 70	LF356H	Samples
LF356H/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	0 to 70	LF356H	Samples
LF356M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LF356 M	
LF356M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LF356 M	Samples
LF356MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	LF356 M	
LF356MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LF356 M	Samples
LF356N	NRND	PDIP	P	8	40	TBD	Call TI	Call TI	0 to 70	LF 356N	
LF356N/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LF 356N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

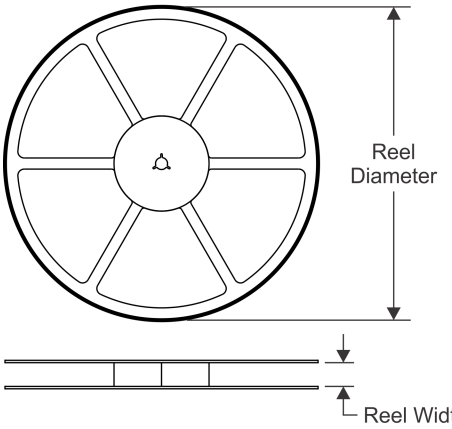
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

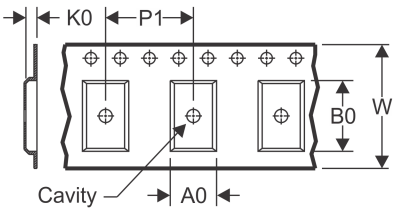
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

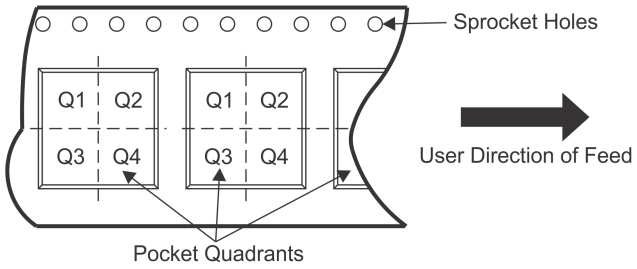


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

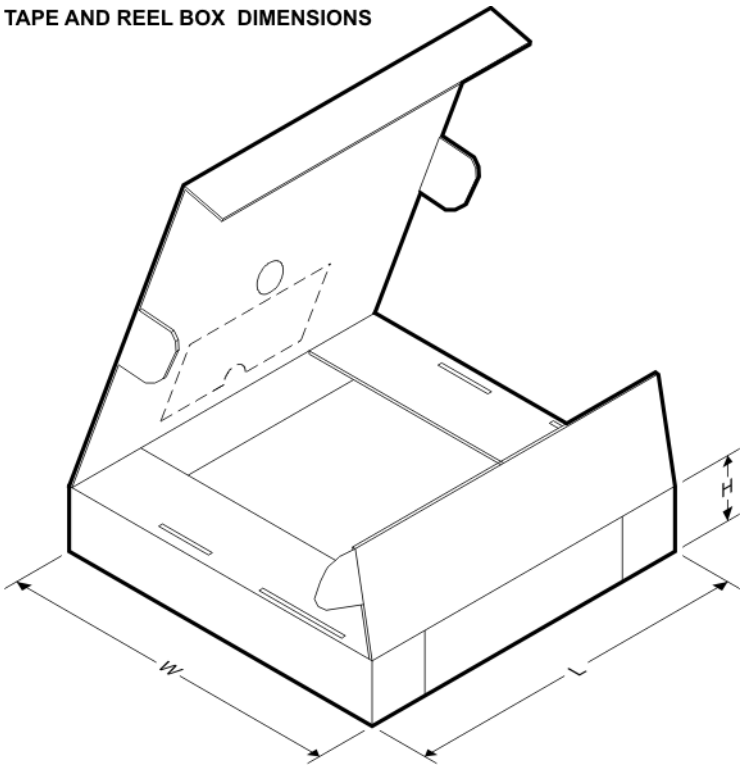
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF356MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LF356MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

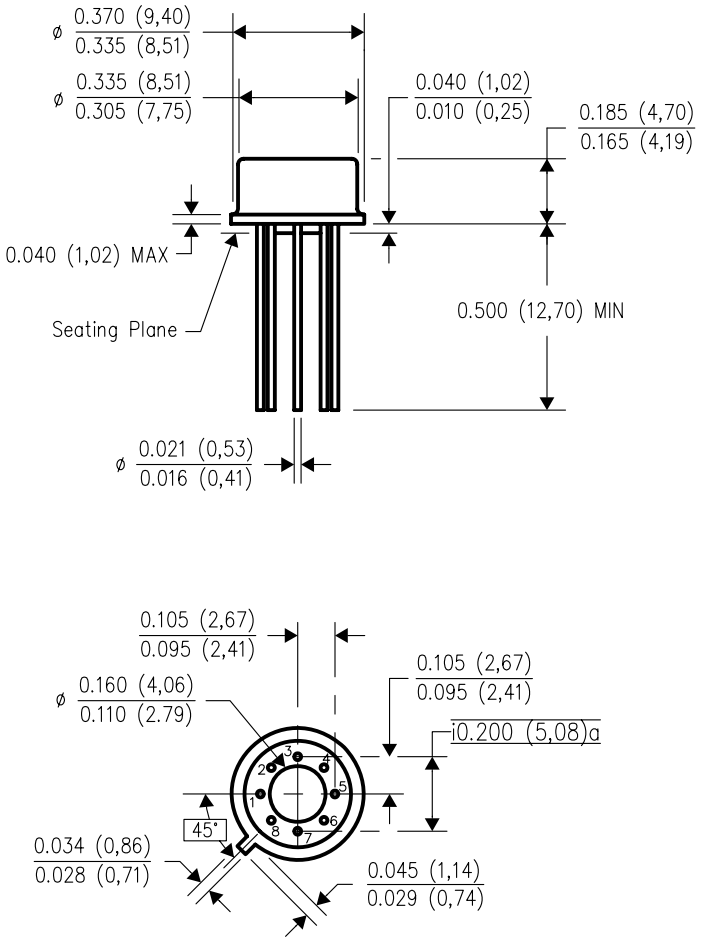
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF356MX	SOIC	D	8	2500	367.0	367.0	35.0
LF356MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE



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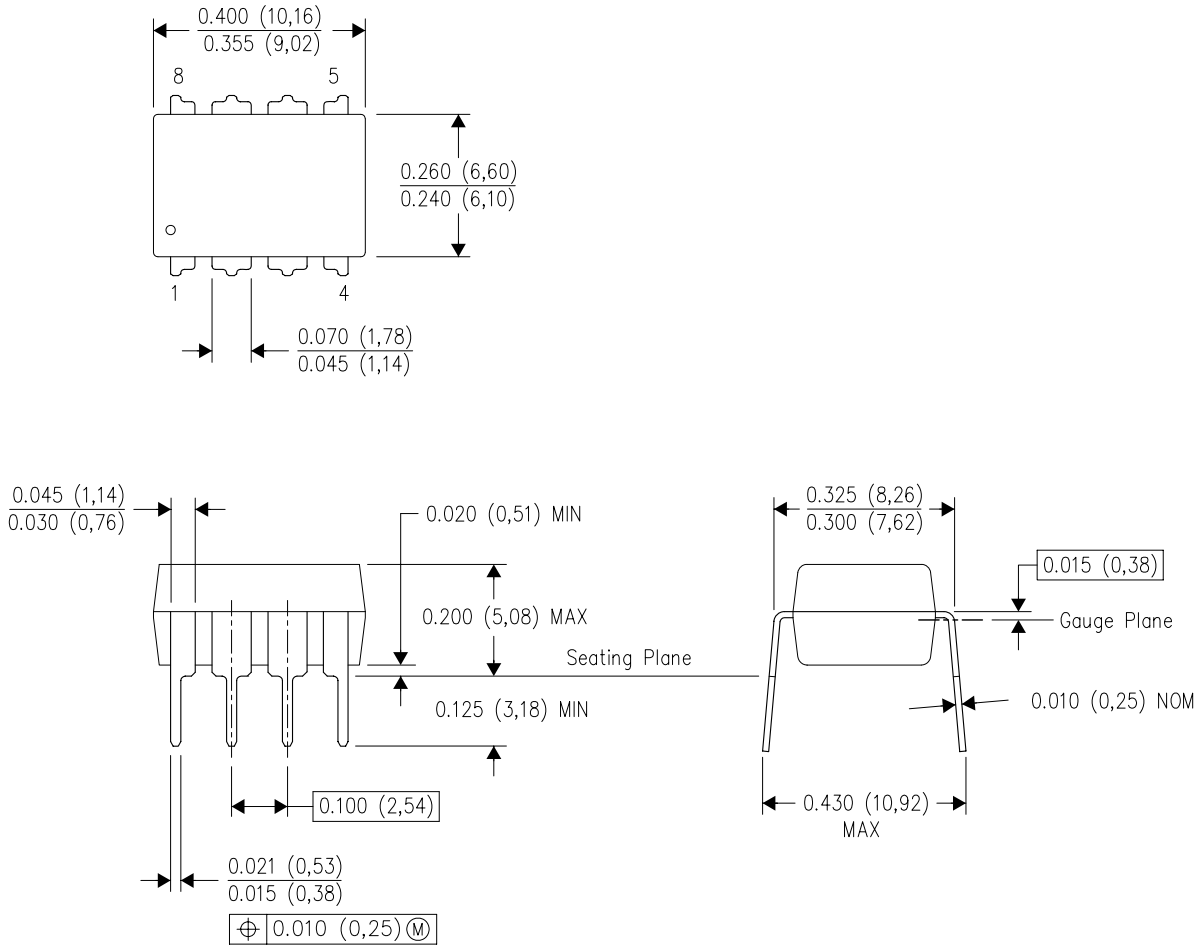
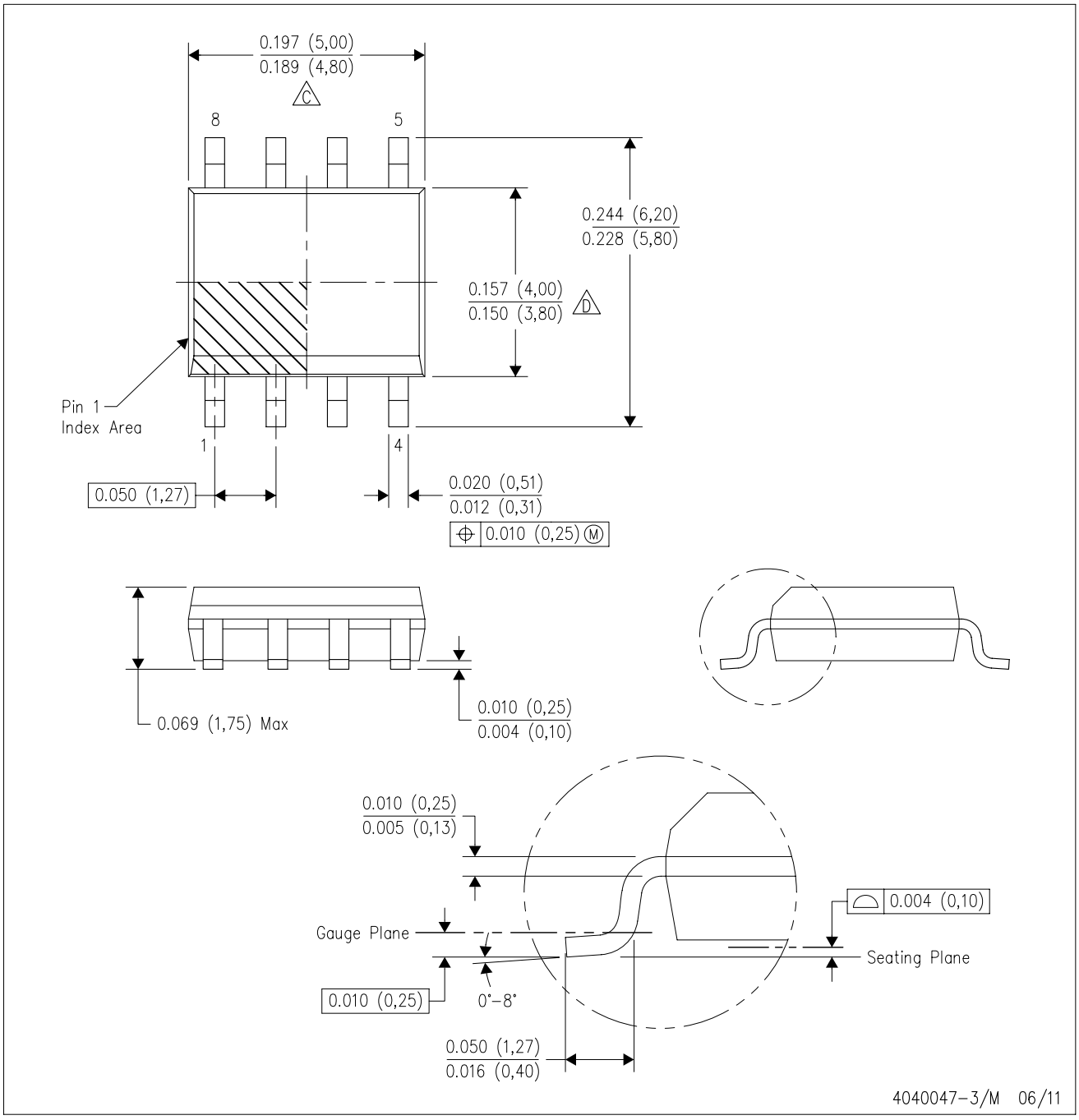
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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